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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,596	12/31/2001	Howard S. David	42390.P13873	2205

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EXAMINER	
LI, ZHUO H	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 03/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding..

Office Action Summary	Application No.	Applicant(s)	
	10/039,596	DAVID, HOWARD S.	
	Examiner	Art Unit	
	Zhuo H. Li	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9,11,12 and 16-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9,11,12 and 16-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office action is in response to the amendment filed 1/9/2006. Accordingly, claims 1-8, 10, 13-15 are canceled and claims 9, 11-12 and 16-25 are pending for examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claim 23 is rejected under 35 U.S.C. 102(b) as being anticipated by Palanca et al. (US PAT. 6,223,258 hereinafter Palanca).

Regarding claim 23, Palanca discloses a system memory (100, figure 1) comprising at least two memory modules (110ı through 110p, figure 1), each module including at least one memory device (215, figure 3) and a data cache (320, figure 3) coupled to the an eviction buffer (340, figure 3), both coupled to the memory device (col. 3 lines 64 through col. 4 line 61 and col. 9 lines 52-56).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 20-22 and 24-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Palanca et al. (US PAT. 6,223,258 hereinafter Palanca) in view of Akkary et al. (US PAT. 5,526,510 hereinafter Akkary).

Regarding claim 20, Palanca discloses a system memory (100, figure 1) comprising at least two memory modules (110i through 110p, figure 1), each module including at least one memory device (215, figure 3) and a data cache (320, figure 3) coupled to the an eviction buffer (340, figure 3), both coupled to the memory device (col. 3 lines 64 through col. 4 line 61 and col. 9 lines 52-56). Palanca differs from the claimed invention in not specifically teaching the memory module to receive a write back command, the write back command to cause a previous line of data, evicted from the data cache and stored within the eviction buffer, to be written out of the eviction buffer to the memory device. However, Akkary teaches in a data cache system comprising a plurality of cache banks (318, figure 2) and a write back buffer (322, figure 2) both coupled to the system memory via a system bus (308, figure 2) to perform memory operation in responds to an instruction from a central processing unit, wherein the write back buffer is capable of temporary storing the eviction entry from the cache bank, and further write back to a main memory such that a pervious line of data evicted from the data cache and stored within the

write back buffer is written out of the write back buffer to the main memory (col. 6 lines 11-20 and lines 34-67). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Palanca in having the memory module to receive a write back command, the write back command to cause a previous line of data, evicted from the data cache and stored within the eviction buffer, to be written out of the eviction buffer to the memory device, as per teaching of Akkary, because it avoids coherency problems and performs replace operation more quickly.

Regarding claim 21, Akkary disclose the data cache to evict previous line of data from the data cache into the write back buffer according to an eviction signal received from the memory controller (col. 6 lines 12-20 and col. 6 line 34 through col. 8 line 27).

Regarding claim 22, Akkary discloses the write back command including way information and bank address information (col. 7 line 48 through col. 8 line 16).

Regarding claims 24-25, the limitations of the claims are rejected as the same reasons as set forth in claim 20.

6. Claims 9 and 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stracovsky et al. (US PAT. 6,378,049 hereinafter Stracovsky) in view of Palanca et al. (US PAT. 6,223,258 hereinafter Palanca) and Akkary et al. (US PAT. 5,526,510 hereinafter Akkary).

Regarding claim 9, Stracovsky discloses a system (100, figure 1B) comprising a processor (102, figure 1B), a memory controller (104, figure 1B) coupled to the processor, the memory controller including an array of tag address storage locations (114, figure 1B) and a command sequencer and serializer unit (116, figure 1B) coupled to the array of tag address

storage locations and a system memory (108, figure 1B) coupled to the memory controller (col. 6 lines 17-45). Stracovsky differs from the claimed invention in not specifically teaching the system memory including at least two memory modules, each memory modules including at least one memory device and a data cache coupled to an eviction buffer, both coupled to the memory device. However, Palanca discloses a system memory (100, figure 1) comprising at least two memory modules (110i through 110p, figure 1), each module including at least one memory device (215, figure 3) and a data cache (320, figure 3) coupled to the an eviction buffer (340, figure 3), both coupled to the memory device (col. 3 lines 64 through col. 4 line 61 and col. 9 lines 52-56) in order to efficiently read non-reusable data from external memory without polluting cache memory. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Stracovsky in having the system memory including at least two memory modules, each memory modules including at least one memory device and a data cache coupled to an eviction buffer, both coupled to the memory device, as per teaching of Palanca, in order to the system memory including at least two memory modules, each memory modules including at least one memory device and a data cache coupled to an eviction buffer, both coupled to the memory device, Furthermore, neither Stracovsky nor Palanca specifically discloses the data cache controlled by a plurality of command delivered by the memory controller and the memory controller writing a current line of data to data cache and the memory controller to further instruct the data cache to evict a previous line of data from the data cache into the eviction buffer. However, Akkary teaches in a data cache system comprising a plurality of cache banks (318, figure 2) and a write back buffer (322, figure 2) both coupled to the system memory via a system bus (308, figure 2) to perform memory operation in responds to

an instruction from a central processing unit, wherein the write back buffer is capable of temporary storing the eviction entry from the cache bank, and further write back to a main memory such that a pervious line of data evicted from the data cache and stored within the write back buffer is written out of the write back buffer to the main memory (col. 6 lines 11-20 and lines 34-67). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combination of Sttraccovsky and Palanca in having the data cache controlled by a plurality of command delivered by the memory controller and the memory controller writing a current line of data to data cache and the memory controller to further instruct the data cache to evict a previous line of data from the data cache into the eviction buffer, as per teaching of Akkary, because it avoids coherency problems and performs replace operation more quickly.

Regarding claim 11, Akkarray discloses the memory controller to deliver a write back command to the data cache, the write back command to cause the previous line of the data to be written out of the eviction buffer to the memory device (col. 6 lines 12-20 and col. 6 lines 34 through col. 8 line 27).

Regarding claim 12, Akkary discloses the write back command including way information and bank address information (col. 7 line 48 through col. 8 line 16).

7. Claims 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stracovsky et al. (US PAT. 6,378,049 hereinafter Stracovsky) in view of Akkary et al. (US PAT. 5,526,510 hereinafter Akkary).

Regarding claim 16, Stracovsky discloses a memory controller (104, figure 1B) comprising an array of tag address storage locations (114, figure 1B) and a command sequencer and serializer unit (116, figure 1B) coupled to the array of tag address storage locations and a system memory (108, figure 1B) coupled to the memory controller (col. 6 lines 17-45). Stracovsky differs from the claimed invention in not specifically teaching the command sequencer and serializer unit to control a data cache and an eviction buffer located on at least one memory modules of system memory to deliver a write back command to the eviction buffer associated with the memory module, the write back command to cause a previous line of data evicted from the data cache and stored in the eviction buffer, to be written out to a memory device of the memory module. However, Akkary teaches in a data cache system comprising a plurality of cache banks (318, figure 2) and a write back buffer (322, figure 2) both coupled to the system memory via a system bus (308, figure 2) to perform memory operation in responds to an instruction from a central processing unit, wherein the write back buffer is capable of temporary storing the eviction entry from the cache bank, and further write back to a main memory such that a pervious line of data evicted from the data cache and stored within the write back buffer is written out of the write back buffer to the main memory (col. 6 lines 11-20 and lines 34-67). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Straccovsky in having the command sequencer and serializer unit to control a data cache and an eviction buffer located on at least one memory modules of system memory to deliver a write back command to the eviction buffer associated with the memory module, the write back command to cause a previous line of data evicted from the data cache and stored in the eviction buffer, to be written out to a memory device of the

memory modul, as per teaching of Akkary, because it avoids coherency problems and performs replace operation more quickly.

Regarding claims 17-18, Akkary discloses the memory controller issuing an eviction signal to the data cache to evict the previous line of data from the data cache into the eviction buffer, and also issuing the write back command to cause the previous line of data to be written out of the eviction buffer to the memory device once the memory device is idle (col. 6 lines 12-20 and col. 6 line 34 through col. 8 line 27).

Regarding claim 19, Akkary discloses the command sequencer and serializer unit, i.e., CPU, to cause a current line of data to be written from the command sequencer and serializer unit to the data cache via the fill buffer (320, figure 2), the command sequencer and serializer unit to cause the previous line of data to be evicted out of the data cache to the eviction buffer, i.e., write back buffer (322, figure 2) located on the memory module (col. 6 line 12 through col. 8 line 27).

Response to Arguments

8. Applicant's arguments with respect to claims 9, 11-12 and 16-25 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H. Li whose telephone number is (571) 272-4183. The examiner can normally be reached on Tue-Fri 7:30 AM-5:00 PM, and alternate Monday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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